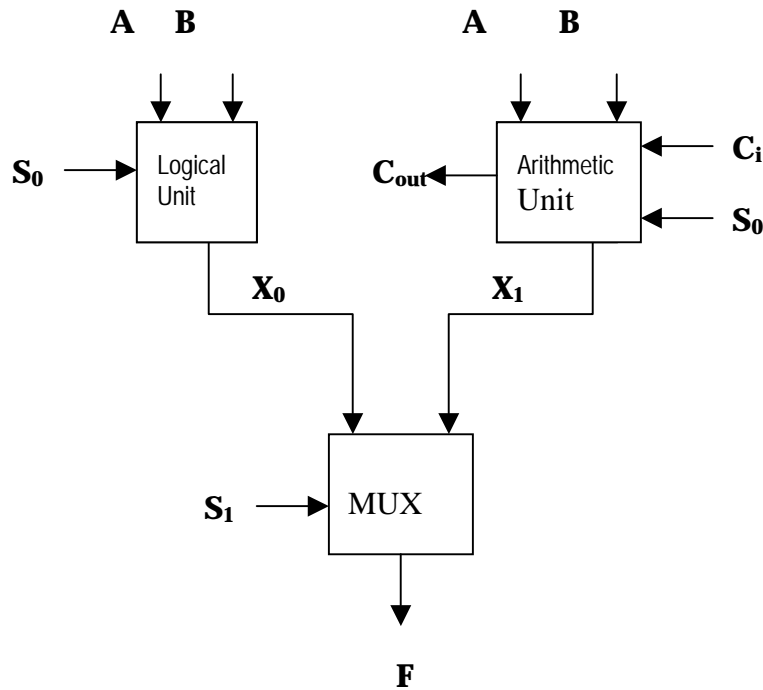


Build a 1-bit ALU that can be cascaded into an n-bit ALU that has the following properties and functions:

- a. All numbers are 2's complement,
- b. Four functions:
  - i.  $S_1S_0=00$  :  $A=B$
  - ii.  $S_1S_0=01$  :  $(AB)' = \text{NAND}(A,B)$
  - iii.  $S_1S_0=10$  :  $-A$
  - iv.  $S_1S_0=11$  :  $A$  plus  $B$
- c. Contains only NAND, XOR, and INVERTER gates

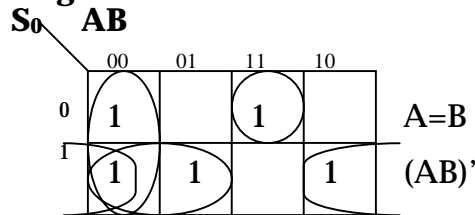
Note that both logical functions (equal and NAND) have  $S_1 = 0$ , and both arithmetic functions have  $S_1 = 1$ . Hence, it's easy to divide these into two units and use a MUX with  $S_1$  as the select line to choose between them.



For the MUX:

This is just a 2-1 MUX where  $F = S'_1X_0 + S_1X_1$

For the Logical Unit:



$$X_0 = A'B' + B'S_0 + ABS'_0 + A'S_0$$

For the arithmetic unit:

Using a full adder we can get  $(-A)$  by taking  $A'$  and adding one (1). Hence, the arithmetic unit is simply a full adder with some logic to control the inputs to give  $(A \text{ plus } B)$  or  $(-A)$

For the negation of A:  $A'$  plus 0 plus 1

For the sum of A and B:  $A \text{ plus } B \text{ plus } C_{in}$

For the full adder, we know

$$S = X \oplus Y \oplus C_{in}$$

$$C_{out} = XY + XC_{in} + YC_{in}$$

Now we need some logic to select the values of X and Y to make our two functions work.

Let the X input be A or A' based on  $S_0$ :

$$X = S'_0A' + S_0A = (S_0 \oplus A)'$$

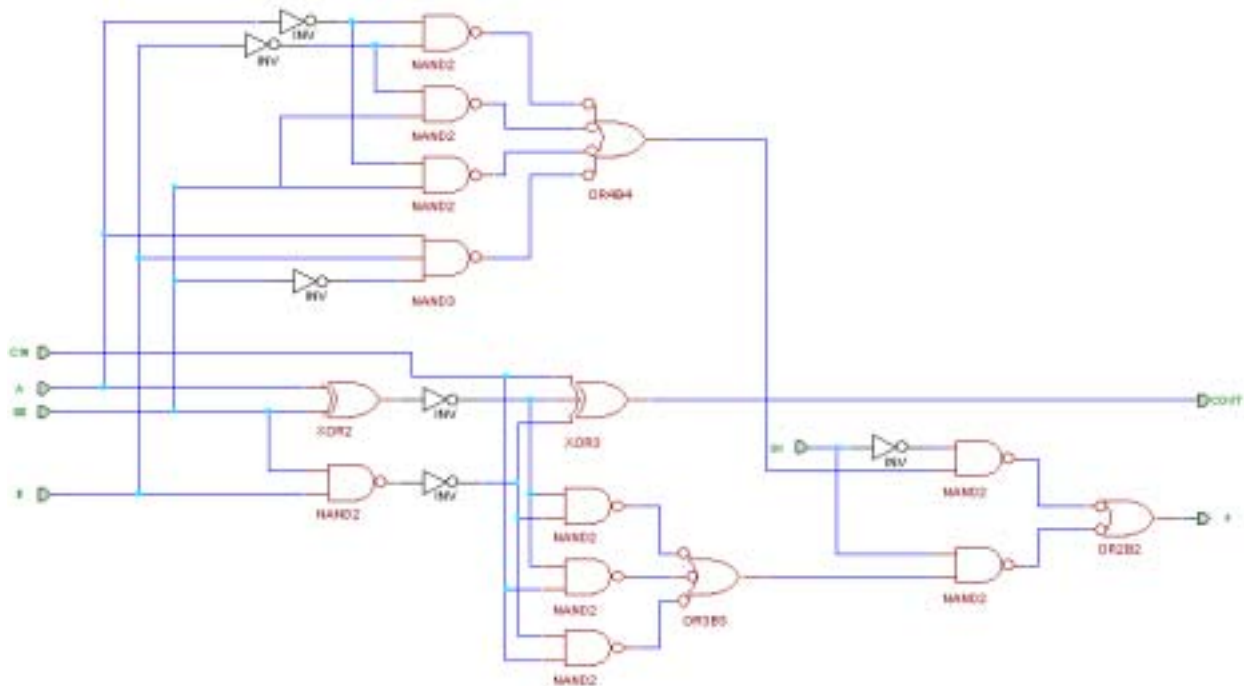
Let the Y input be 0 or B based on  $S_0$ :

$$Y = S_0B$$

The addition of 1 for the negation will be done through  $C_{in}$  when  $S_0 = 0$

$$C_{in} = S'_0$$

The complete circuit looks like this:



If this is the least significant bit, then  $C_{in}$  should be  $S'_0$ . This is the general circuit, however, where  $C_{in}$  of stage  $n$  is wired to  $C_{out}$  of stage  $n-1$ .