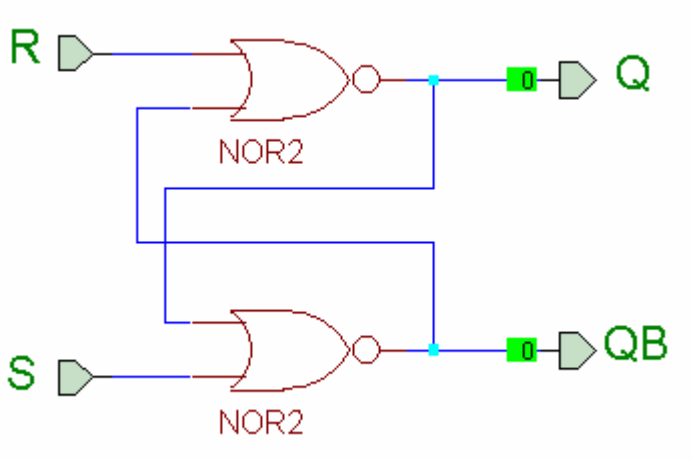
CSE 260M - Homework 8

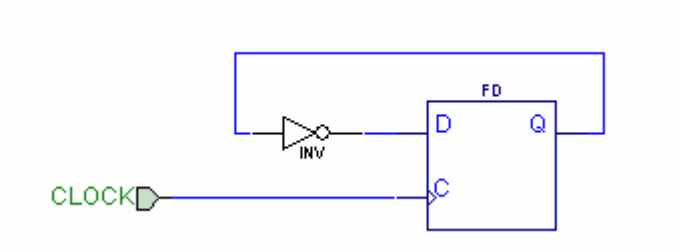
Due November 1, 2006

1. Draw a timing diagram for the following NOR circuit for an SR latch with the following input changes. Assume a 2.5 ns delay for each gate. Comment on why we don't let S=R=1 on a latch. Show your timing diagram to at least 60 ns.

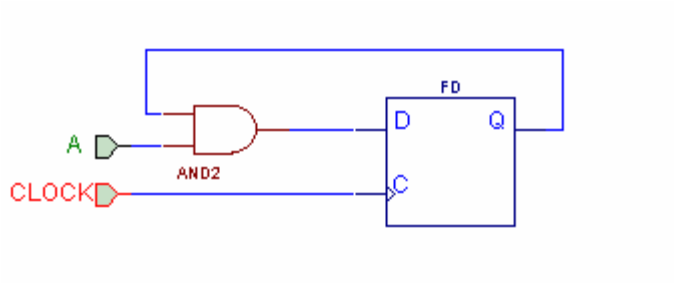


2. Assume that each flip-flop has a setup time of 2 ns, a hold time of 3 ns and a clock-to-output delay of 5 ns. Further assume that each gate has a delay of 2 ns except each inverter has a delay of 1 ns. What is the maximum clock frequency that you can clock the following circuits. Also discuss what constraints are placed on the inputs.

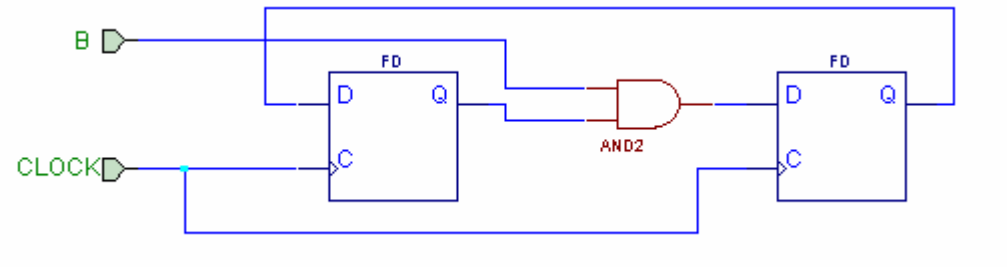
a.



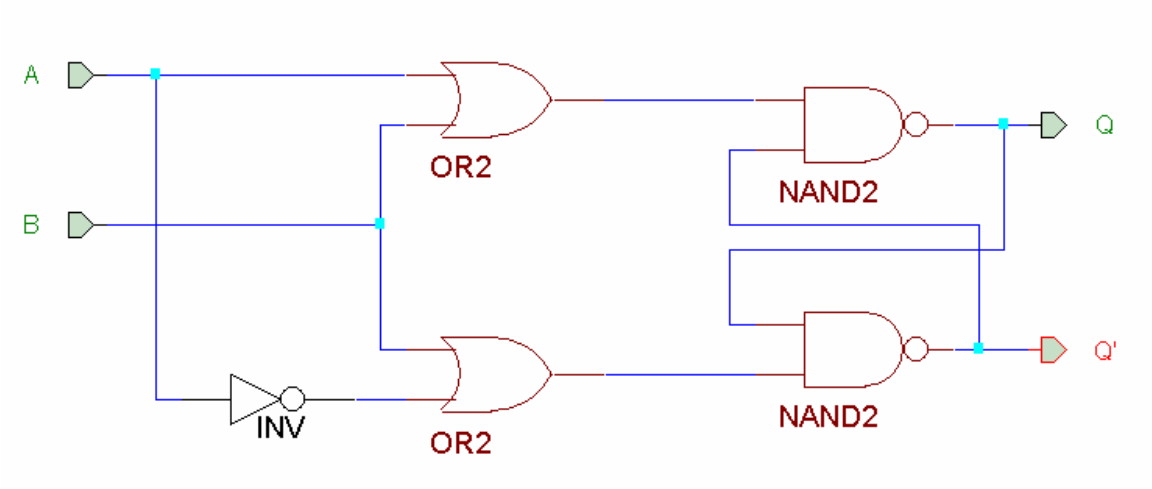
b.



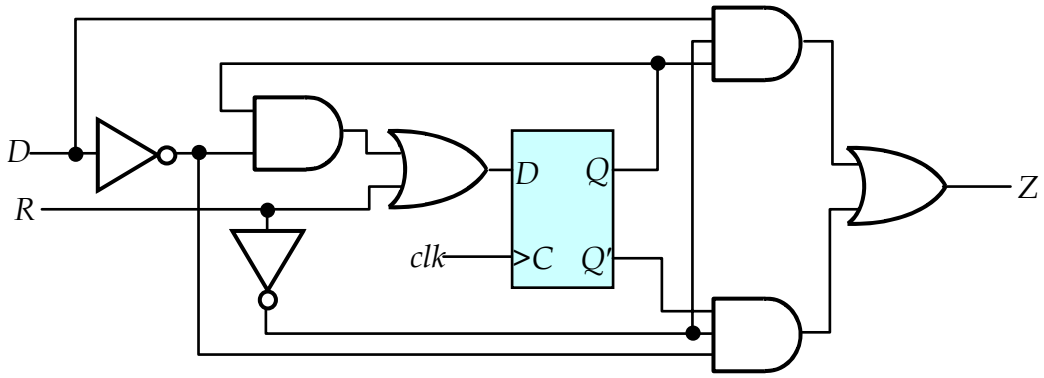
c.



3. For the following storage device, derive the state transition diagram (bubble diagram) and find the characteristic equation (note the outputs **are** complements of each other).



4. Derive a state transition diagram for the sequential circuit shown below. Give a set of test inputs for this circuit that will verify every transition in the state diagram (including "self-loops").



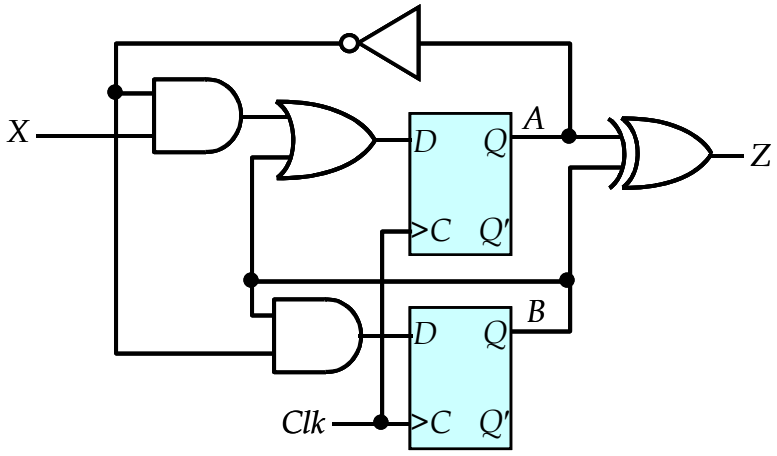
5. A sequential circuit with two *D* flip flops *A* and *B* and two inputs *X* and *Y* and one output *Z* is specified by the following equations.

$$D_A = X'Y + XA \qquad D_B = X'B + XA \qquad Z = XB$$

(a) Draw the logic diagram of the circuit, (b) Derive the state table and (c) Derive the state diagram.

6. Derive a state diagram and state table for a circuit with one input and one output whose output will be high if the input stream has the pattern 10110. (The pattern 10110 has a 1, then a 0, then a 1, etc., in time. The left-most bit is first, in other words.). The patterns could overlap. You should detect these patterns, too. Use a Mealy machine.

Consider the sequential circuit shown below. Assume that the flip flops have a setup time of 2 ns, a hold time of 1 ns and a propagation delay between 1 and 3 ns. Also assume that the maximum clock skew is 1 ns and that all the gates have a propagation delay between .5 and 2 ns. What is the shortest clock period for which we can be certain that there are no violations of setup times, assuming no changes at the input *X*? Is the circuit subject to hold time violations? If so, what would you do to eliminate the hold time violations? If the clock goes high at time 0, during what time period must *X* be stable to ensure that there are no violations of setup and hold times? During what time period is it possible for the output to be changing. If the clock could change anytime between *t*=-1 ns and *t*=+1 ns, how do the last two answers change?



7. Design a sequential circuit that determines if the number of 1s in an input data stream is divisible by 3 or not. Your circuit will have a data input *D*, an enable input *EN* and a clock input. It will also have a single output Z. When *EN* = 0, *Z*=1. After *EN* goes high, your circuit will observe the number of 1s in the incoming data stream and whenever the number of 1s seen so far is divisible by 3, the output *Z*, will be 1. At all other times it will be zero. The serial parity generator on page 4-7 of the notes performs a similar function. **Create a state transition diagram for your circuit. Find the output equation and the next state equations.**