CSE 260M - Homework 6

Due October 11, 2006

1. A combinational circuit is defined by the following three Boolean functions.

   $F_1 = (X+Y)' + XYZ'$
   $F_2 = (X+Y)' + X'YZ$
   $F_3 = XYZ + (X+Y)'$

   Implement each using only 4-1 muxes. You may assume you have complemented and uncomplemented inputs.

2. Implement a Half Adder in a Xilinx XC3S50-5 Spartan 3 FPGA (in the PQ208 package) using (a) a schematic-based approach, and (b) a VHDL-based approach. For part (a), turn in your schematic, a simulation showing that your circuit works properly, and a printout of the place-and-route report. For part (b), turn in your VHDL, a simulation showing that the circuit works properly, and a printout of the place-and-route report.

3. Assume you have a 4-bit full adder that you want to use for adding 2's complement numbers. Develop an equation for *V*, the overflow flag, that will give an output of a 1 when the addition results in an overflow condition. Overflow is defined as a case where the result is too positive or too negative to be represented in 4-bit 2's complement format.

4. Design a circuit that determines if the 4-bit binary input is equal to one or greater than five.

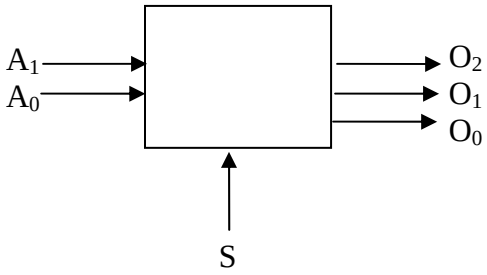
5. In the equation below, the function *greater_than*($x_3x_2x_1x_0$,$z_3z_2z_1z_0$) is true, if and only if, the numerical value represented by $x_3x_2x_1x_0$ is greater than the numerical value represented by $z_3z_2z_1z_0$. Similarly for the *equal* function. Explain why this equation is true.

$$greater\_than(x_3x_2x_1x_0, z_3z_2z_1z_0) = greater\_than(x_3x_2x_1, z_3z_2z_1) + x_0z_0'equal(x_3x_2x_1, z_3z_2z_1)$$

   Use this equation to design a 4 bit comparison circuit consisting of four copies of a single sub-circuit. Your circuit should have three outputs $X>Z$, $X=Z$ and $X<Z$, where the first output is high if the numerical value represented by inputs $x_3x_2x_1x_0$ is greater than the numerical value represented by inputs $z_3z_2z_1z_0$, and so forth.

Assuming a 1 ns gate delay on all gates in your design, what is the circuit's worst-case propagation delay?

6. Determine the output equations for a circuit that will either add one or add two to a 2-bit binary based on a select line (S=0, increment by one; S=1, increment by 2):



7. The logic diagram below shows a 5 bit ripple-carry decrement circuit. Draw a logic diagram for a 5 bit borrow-lookahead decrement circuit. You may use gates with more than 2 inputs. What is the worst-case propagation delay for your circuit if all gates with 1 input have a delay of 1 ns, all gates with 2 inputs have a delay of 2 ns, all gates with 3 or 4 inputs have a delay of 4 ns and all gates with 5 to 8 inputs have a delay of 6 ns?