

CSE 260M – Design Problem 3

Due December 6, 2006

Extend your “color bar” generator from Design Problem 2 to display a more elaborate pattern stored in a block RAM inside the Spartan 3 FPGA.

Initialize your pattern in the block RAM using a .coe file when you generate the RAM using CoreGen.

You have flexibility in defining the pattern displayed, but it must be “interesting,” i.e., it cannot be a screen that is all one color. A chess board pattern is an example of a minimum-effort sort of pattern that will be accepted for full credit.

Demonstrate your working design to one of the TAs, and email your vga2.vhd and vga2.mcs files to Dr. Richard prior to class on Wednesday, December 6, 2006.